FIG. 1

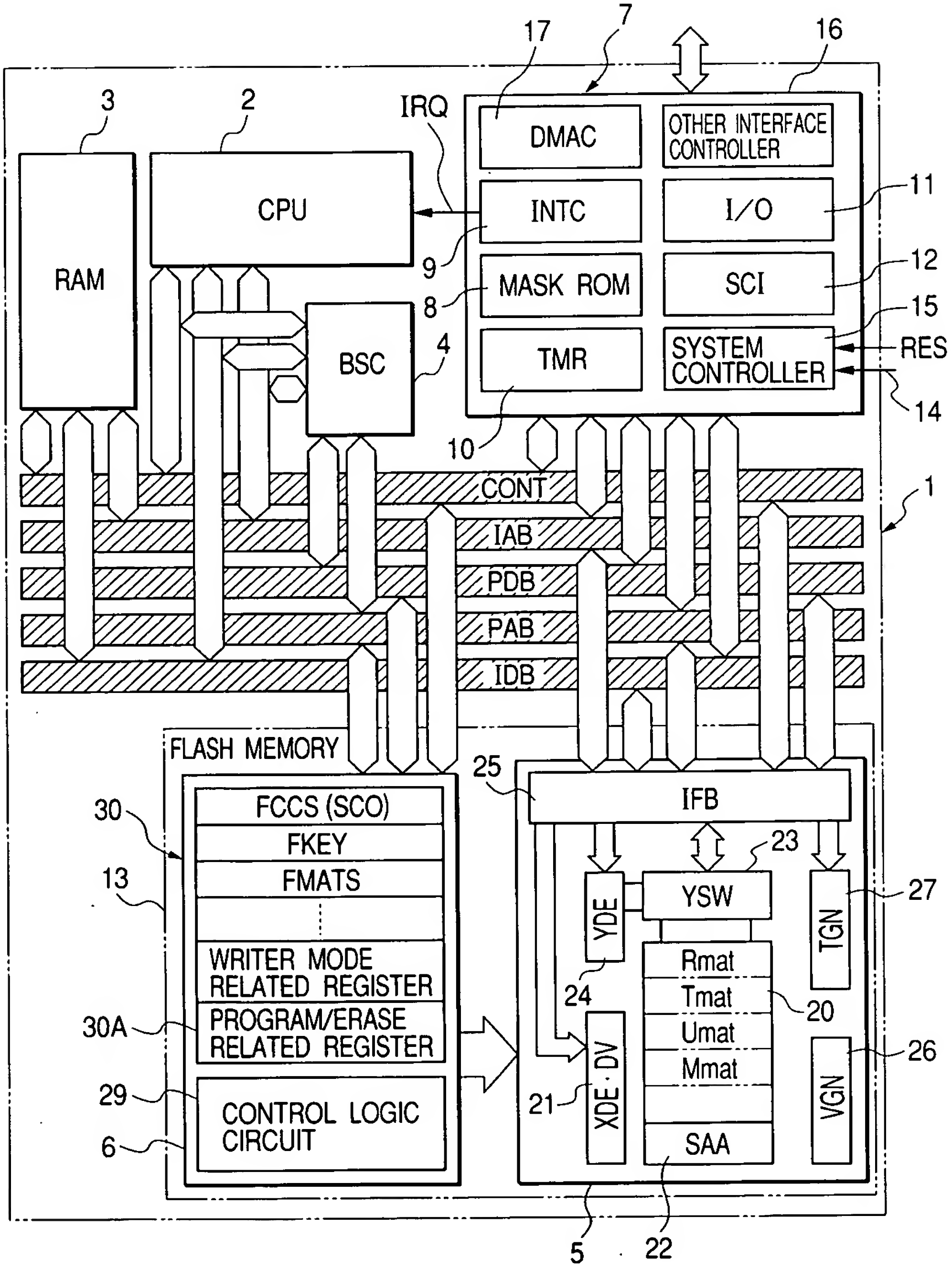

17
7
16
3
2
IRQ
DMAC
OTHER INTERFACE CONTROLLER
RAM
CPU
INTC
I/O
11
9
MASK ROM
SCI
12
8
15
BSC
4
TMR
SYSTEM CONTROLLER
RES
14
10
CONT
1
IAB
PDB
PAB
IDB
FLASH MEMORY
25
IFB
30
FCCS (SCO)
FKEY
13
FMATS
23
YDE
YSW
TGN
27
WRITER MODE RELATED REGISTER
24
Rmat
Tmat
20
Umat
30A
PROGRAM/ERASE RELATED REGISTER
XDE · DV
Mmat
26
VGN
29
21
CONTROL LOGIC CIRCUIT
SAA
6
5
22

FIG. 2

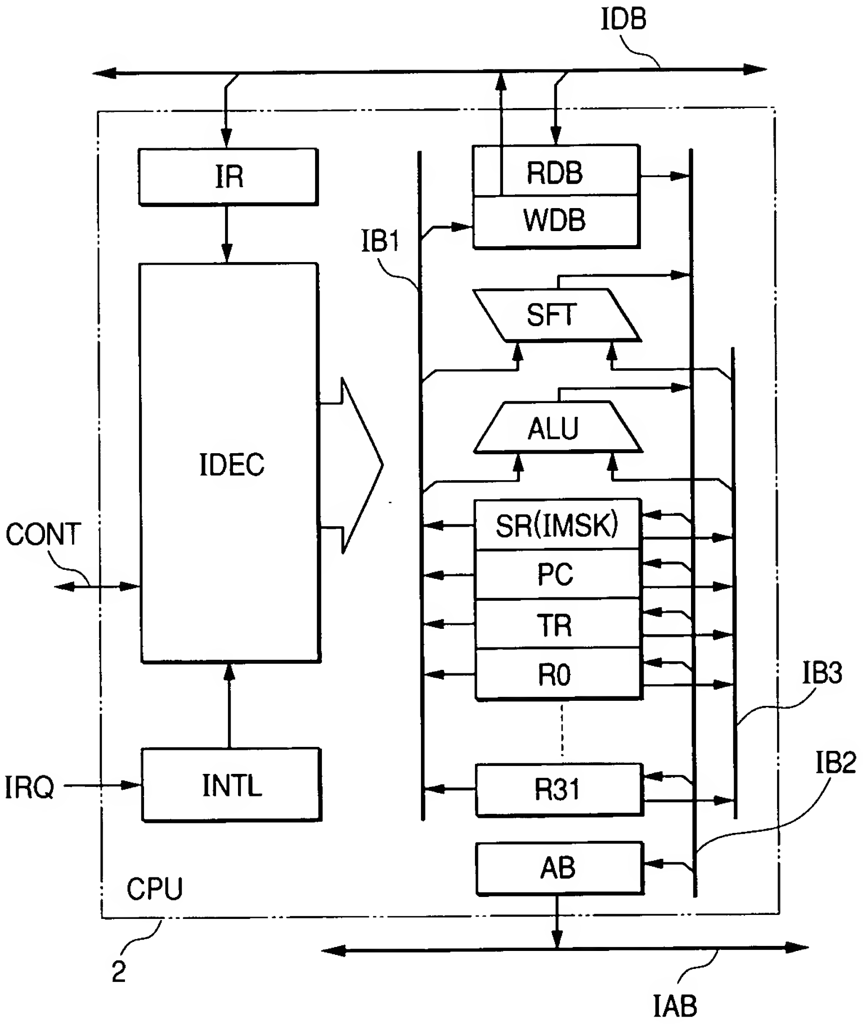

IDB
IR
IDEC
INTL
CONT
IRQ
IB1
RDB
WDB
SFT
ALU
SR(IMSK)
PC
TR
R0
R31
AB
IB3
IB2
CPU
2
IAB

FIG. 3

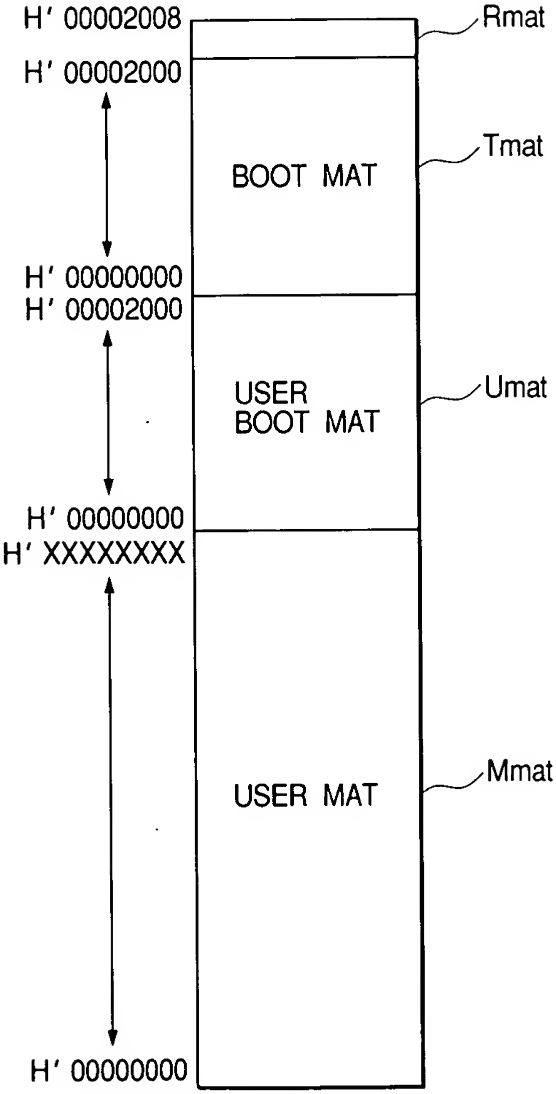

H' 00002008
H' 00002000
H' 00000000
H' 00002000
H' 00000000
H' XXXXXXXX
H' 00000000
BOOT MAT
USER BOOT MAT
USER MAT
Rmat
Tmat
Umat
Mmat

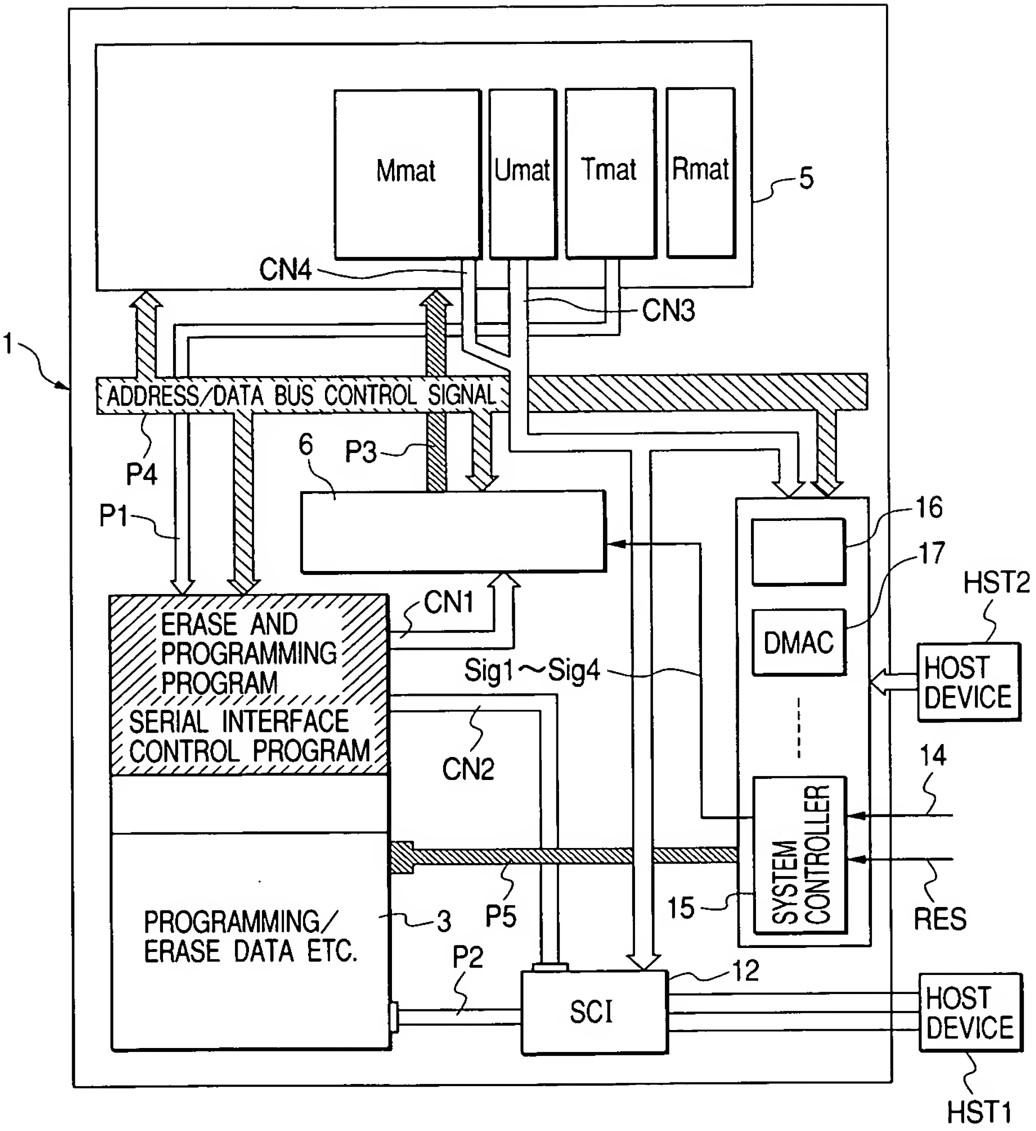
FIG. 4(A)

OPERATION MODE MAT	BOOT MODE			WRITER MODE		
	ACCESS	PROGRAM	ERASE	ACCESS	PROGRAM	ERASE
USER MAT (Mmat)	○	○	○	○	○	○
USER BOOT MAT (Umat)	○	○	○	○	○	○
BOOT MAT (Tmat)	△	×	×	△	×	×
REPAIR & TRIMMING (Rmat)	×	×	×	×	×	×

FIG. 4(B)

OPERATION MODE MAT	USER BOOT MODE			USER MODE		
	ACCESS	PROGRAM	ERASE	ACCESS	PROGRAM	ERASE
USER MAT (Mmat)	○	○	○	○	○	○
USER BOOT MAT (Umat)	○	×	×	○	×	×
BOOT MAT (Tmat)	△	×	×	△	×	×
REPAIR & TRIMMING (Rmat)	×	×	×	×	×	×

FIG. 5



Mmat
Umat
Tmat
Rmat
5
CN4
CN3
1
ADDRESS/DATA BUS CONTROL SIGNAL
P4
P1
6
P3
16
17
HST2
DMAC
HOST DEVICE
CN1
ERASE AND PROGRAMMING PROGRAM
SERIAL INTERFACE CONTROL PROGRAM
Sig1～Sig4
CN2
14
SYSTEM CONTROLLER
PROGRAMMING/ ERASE DATA ETC.
3
P5
15
RES
P2
12
SCI
HOST DEVICE
HST1

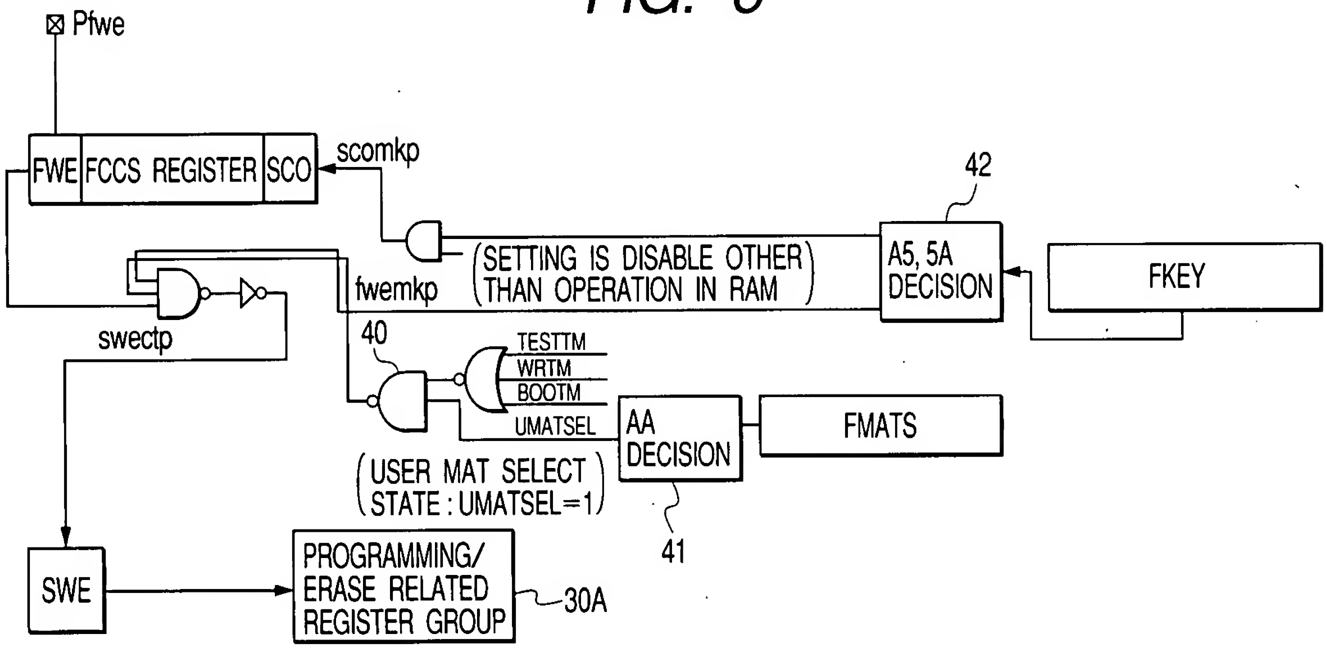

⊠ Pfwe
FWE
FCCS REGISTER
SCO
scomkp
42
A5, 5A DECISION
FKEY
(SETTING IS DISABLE OTHER THAN OPERATION IN RAM)
fwemkp
swectp
40
TESTTM
WRTM
BOOTM
UMATSEL
AA DECISION
FMATS
41
(USER MAT SELECT STATE : UMATSEL=1)
SWE
PROGRAMMING/ ERASE RELATED REGISTER GROUP
30A

FIG. 6

FIG. 7

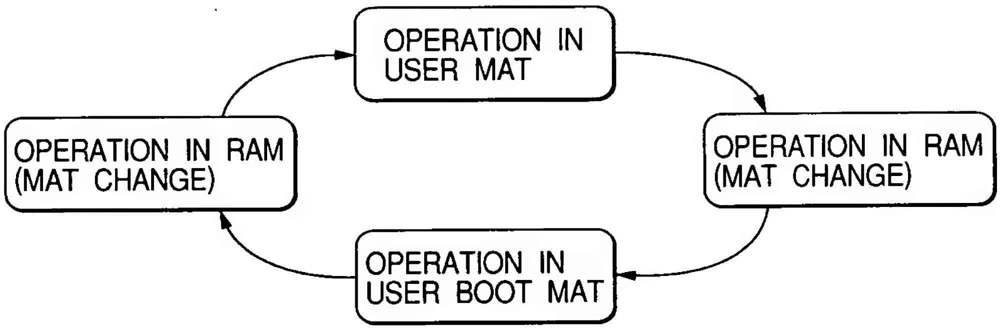

OPERATION IN USER MAT
OPERATION IN RAM (MAT CHANGE)
OPERATION IN USER BOOT MAT
OPERATION IN RAM (MAT CHANGE)

FIG. 8

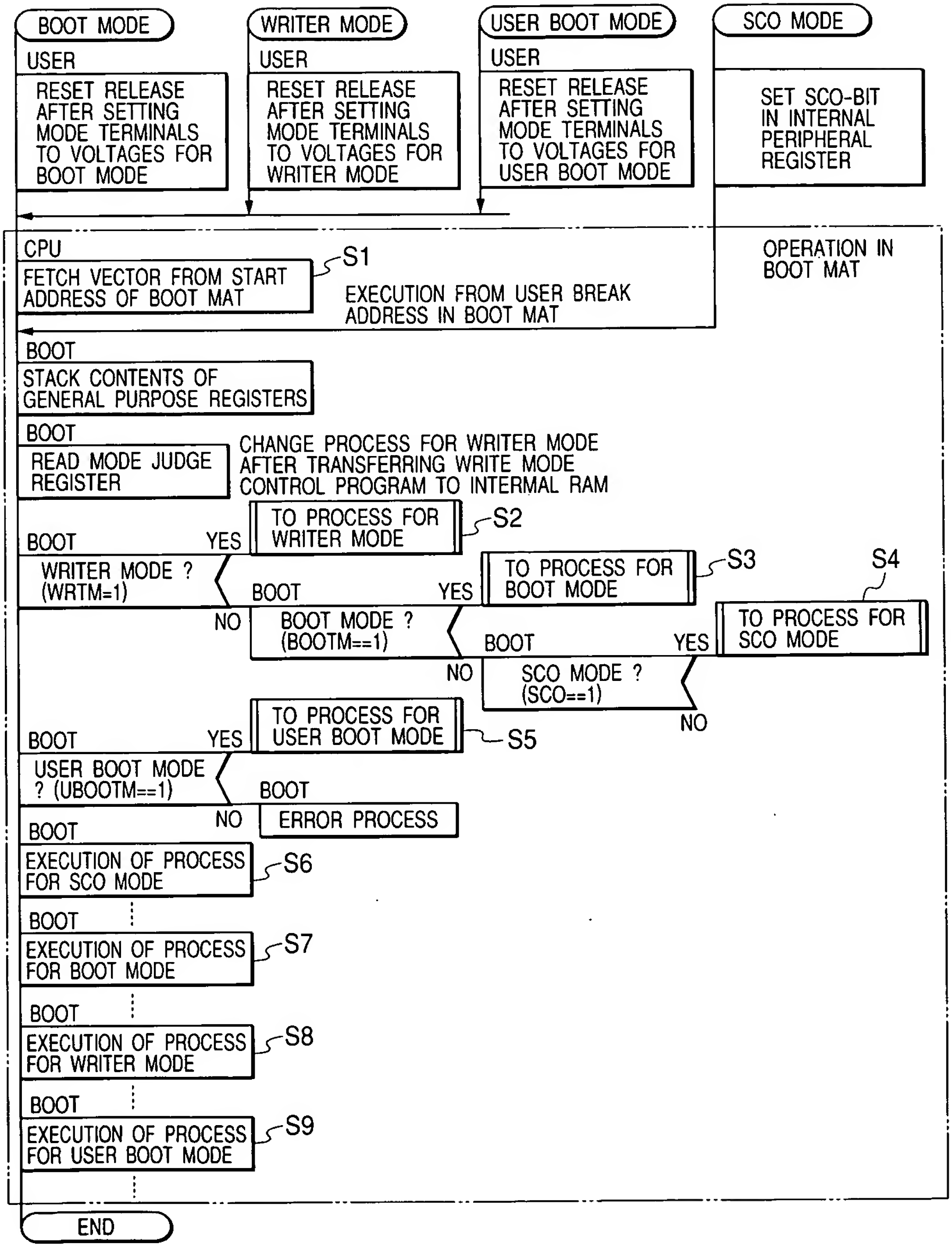

BOOT MODE
USER
RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR BOOT MODE
WRITER MODE
USER
RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR WRITER MODE
USER BOOT MODE
USER
RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR USER BOOT MODE
SCO MODE
SET SCO-BIT IN INTERNAL PERIPHERAL REGISTER
OPERATION IN BOOT MAT
CPU
FETCH VECTOR FROM START ADDRESS OF BOOT MAT
S1
EXECUTION FROM USER BREAK ADDRESS IN BOOT MAT
BOOT
STACK CONTENTS OF GENERAL PURPOSE REGISTERS
BOOT
READ MODE JUDGE REGISTER
CHANGE PROCESS FOR WRITER MODE AFTER TRANSFERRING WRITE MODE CONTROL PROGRAM TO INTERMAL RAM
BOOT
WRITER MODE ? (WRTM=1)
YES
TO PROCESS FOR WRITER MODE
S2
NO
BOOT
BOOT MODE ? (BOOTM==1)
YES
TO PROCESS FOR BOOT MODE
S3
NO
BOOT
SCO MODE ? (SCO==1)
YES
TO PROCESS FOR SCO MODE
S4
NO
BOOT
USER BOOT MODE ? (UBOOTM==1)
YES
TO PROCESS FOR USER BOOT MODE
S5
NO
BOOT
ERROR PROCESS
BOOT
EXECUTION OF PROCESS FOR SCO MODE
S6
BOOT
EXECUTION OF PROCESS FOR BOOT MODE
S7
BOOT
EXECUTION OF PROCESS FOR WRITER MODE
S8
BOOT
EXECUTION OF PROCESS FOR USER BOOT MODE
S9
END

FIG. 9

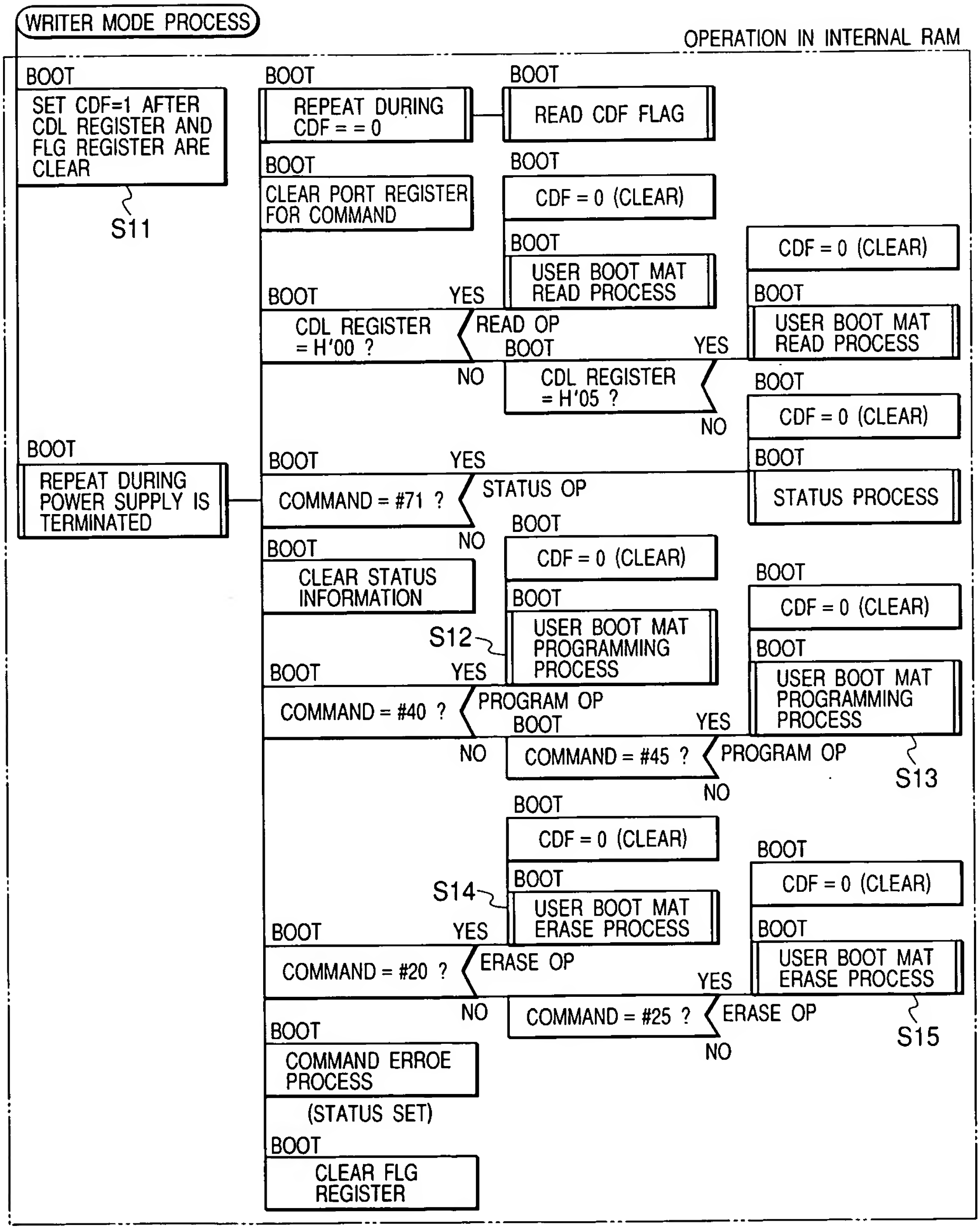

WRITER MODE PROCESS
OPERATION IN INTERNAL RAM
BOOT
SET CDF=1 AFTER CDL REGISTER AND FLG REGISTER ARE CLEAR
S11
BOOT
REPEAT DURING CDF = = 0
BOOT
READ CDF FLAG
BOOT
CLEAR PORT REGISTER FOR COMMAND
BOOT
CDF = 0 (CLEAR)
BOOT
USER BOOT MAT READ PROCESS
CDF = 0 (CLEAR)
BOOT
YES
CDL REGISTER = H'00 ?
READ OP
BOOT
YES
BOOT
USER BOOT MAT READ PROCESS
NO
CDL REGISTER = H'05 ?
NO
BOOT
CDF = 0 (CLEAR)
BOOT
REPEAT DURING POWER SUPPLY IS TERMINATED
BOOT
YES
COMMAND = #71 ?
STATUS OP
BOOT
STATUS PROCESS
NO
BOOT
CDF = 0 (CLEAR)
BOOT
CLEAR STATUS INFORMATION
BOOT
CDF = 0 (CLEAR)
S12
BOOT
USER BOOT MAT PROGRAMMING PROCESS
BOOT
BOOT
YES
USER BOOT MAT PROGRAMMING PROCESS
COMMAND = #40 ?
PROGRAM OP
BOOT
YES
NO
COMMAND = #45 ?
PROGRAM OP
S13
NO
BOOT
CDF = 0 (CLEAR)
BOOT
CDF = 0 (CLEAR)
S14
BOOT
USER BOOT MAT ERASE PROCESS
BOOT
BOOT
YES
USER BOOT MAT ERASE PROCESS
COMMAND = #20 ?
ERASE OP
YES
NO
COMMAND = #25 ?
ERASE OP
S15
NO
BOOT
COMMAND ERROE PROCESS
(STATUS SET)
BOOT
CLEAR FLG REGISTER

FIG. 10

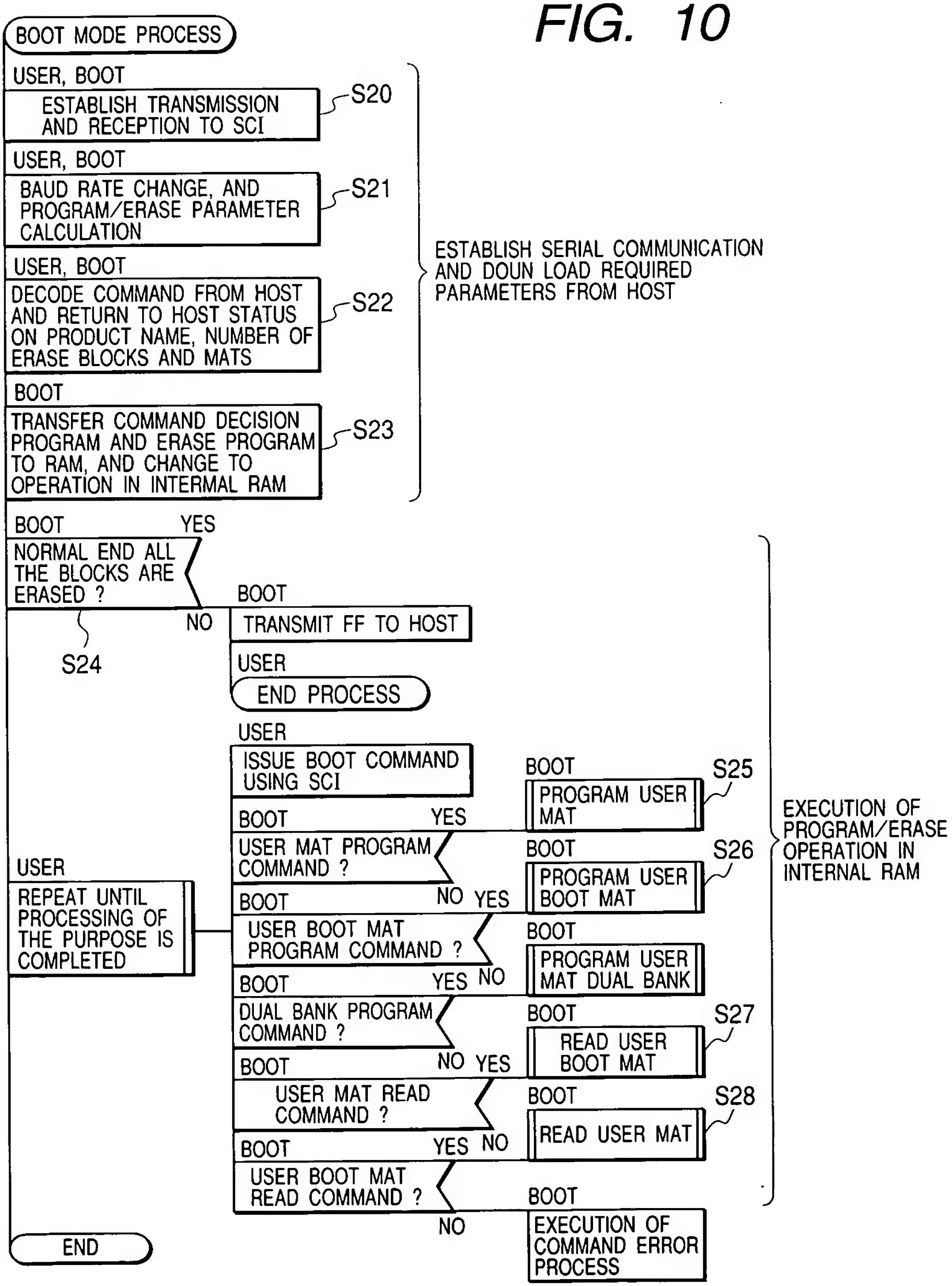

BOOT MODE PROCESS
USER, BOOT
ESTABLISH TRANSMISSION AND RECEPTION TO SCI
S20
USER, BOOT
BAUD RATE CHANGE, AND PROGRAM/ERASE PARAMETER CALCULATION
S21
USER, BOOT
DECODE COMMAND FROM HOST AND RETURN TO HOST STATUS ON PRODUCT NAME, NUMBER OF ERASE BLOCKS AND MATS
S22
BOOT
TRANSFER COMMAND DECISION PROGRAM AND ERASE PROGRAM TO RAM, AND CHANGE TO OPERATION IN INTERMAL RAM
S23
ESTABLISH SERIAL COMMUNICATION AND DOUN LOAD REQUIRED PARAMETERS FROM HOST
BOOT
YES
NORMAL END ALL THE BLOCKS ARE ERASED ?
NO
S24
BOOT
TRANSMIT FF TO HOST
USER
END PROCESS
USER
ISSUE BOOT COMMAND USING SCI
BOOT
YES
USER MAT PROGRAM COMMAND ?
BOOT
PROGRAM USER MAT
S25
NO
YES
BOOT
USER BOOT MAT PROGRAM COMMAND ?
BOOT
PROGRAM USER BOOT MAT
S26
YES
NO
BOOT
DUAL BANK PROGRAM COMMAND ?
BOOT
PROGRAM USER MAT DUAL BANK
NO
YES
BOOT
USER MAT READ COMMAND ?
BOOT
READ USER BOOT MAT
S27
YES
NO
BOOT
USER BOOT MAT READ COMMAND ?
BOOT
READ USER MAT
S28
NO
BOOT
EXECUTION OF COMMAND ERROR PROCESS
USER
REPEAT UNTIL PROCESSING OF THE PURPOSE IS COMPLETED
END
EXECUTION OF PROGRAM/ERASE OPERATION IN INTERNAL RAM

FIG. 11

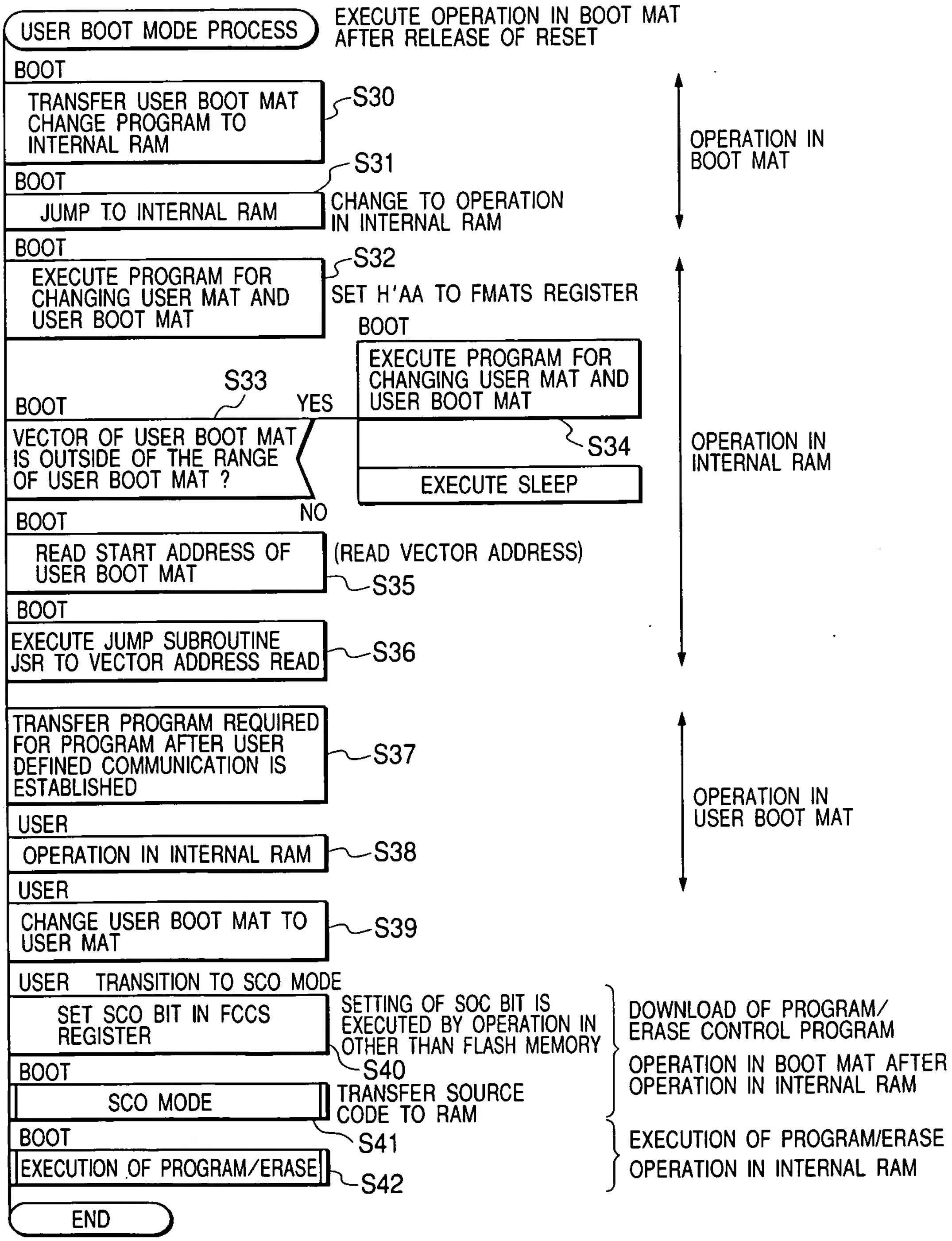

USER BOOT MODE PROCESS
EXECUTE OPERATION IN BOOT MAT AFTER RELEASE OF RESET
BOOT
TRANSFER USER BOOT MAT CHANGE PROGRAM TO INTERNAL RAM
S30
BOOT
JUMP TO INTERNAL RAM
S31
CHANGE TO OPERATION IN INTERNAL RAM
OPERATION IN BOOT MAT
BOOT
EXECUTE PROGRAM FOR CHANGING USER MAT AND USER BOOT MAT
S32
SET H'AA TO FMATS REGISTER
BOOT
EXECUTE PROGRAM FOR CHANGING USER MAT AND USER BOOT MAT
S33
YES
BOOT
VECTOR OF USER BOOT MAT IS OUTSIDE OF THE RANGE OF USER BOOT MAT ?
S34
EXECUTE SLEEP
NO
OPERATION IN INTERNAL RAM
BOOT
READ START ADDRESS OF USER BOOT MAT
(READ VECTOR ADDRESS)
S35
BOOT
EXECUTE JUMP SUBROUTINE JSR TO VECTOR ADDRESS READ
S36
TRANSFER PROGRAM REQUIRED FOR PROGRAM AFTER USER DEFINED COMMUNICATION IS ESTABLISHED
S37
USER
OPERATION IN INTERNAL RAM
S38
OPERATION IN USER BOOT MAT
USER
CHANGE USER BOOT MAT TO USER MAT
S39
USER TRANSITION TO SCO MODE
SET SCO BIT IN FCCS REGISTER
SETTING OF SOC BIT IS EXECUTED BY OPERATION IN OTHER THAN FLASH MEMORY
S40
DOWNLOAD OF PROGRAM/ ERASE CONTROL PROGRAM
OPERATION IN BOOT MAT AFTER OPERATION IN INTERNAL RAM
BOOT
SCO MODE
TRANSFER SOURCE CODE TO RAM
BOOT
S41
EXECUTION OF PROGRAM/ERASE
S42
EXECUTION OF PROGRAM/ERASE
OPERATION IN INTERNAL RAM
END

FIG. 12

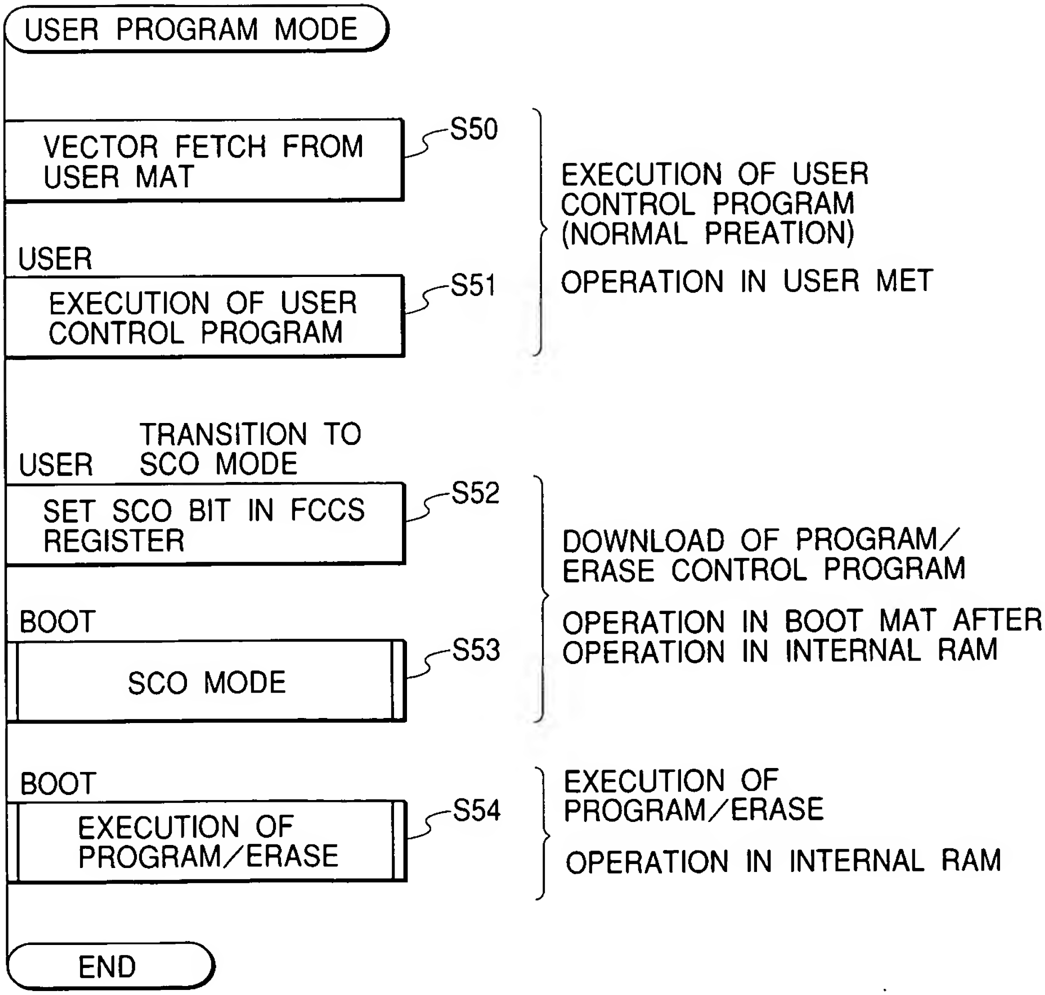

USER PROGRAM MODE
VECTOR FETCH FROM USER MAT
S50
USER
EXECUTION OF USER CONTROL PROGRAM
S51
EXECUTION OF USER CONTROL PROGRAM (NORMAL PREATION)
OPERATION IN USER MET
USER
TRANSITION TO SCO MODE
SET SCO BIT IN FCCS REGISTER
S52
BOOT
SCO MODE
S53
DOWNLOAD OF PROGRAM/ ERASE CONTROL PROGRAM
OPERATION IN BOOT MAT AFTER OPERATION IN INTERNAL RAM
BOOT
EXECUTION OF PROGRAM/ERASE
S54
EXECUTION OF PROGRAM/ERASE
OPERATION IN INTERNAL RAM
END

FIG. 13

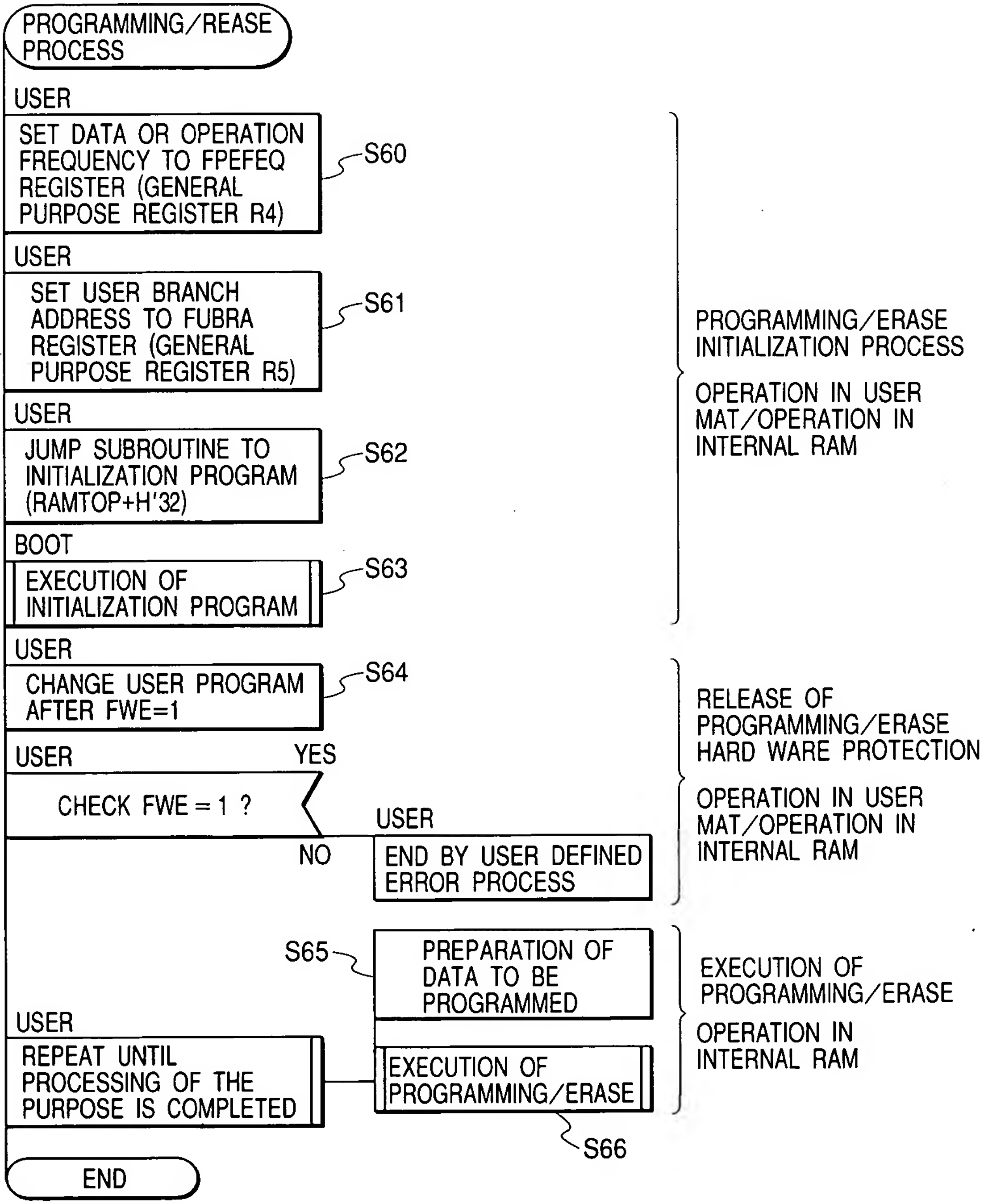

PROGRAMMING/REASE PROCESS
USER
SET DATA OR OPERATION FREQUENCY TO FPEFEQ REGISTER (GENERAL PURPOSE REGISTER R4)
S60
USER
SET USER BRANCH ADDRESS TO FUBRA REGISTER (GENERAL PURPOSE REGISTER R5)
S61
USER
JUMP SUBROUTINE TO INITIALIZATION PROGRAM (RAMTOP+H'32)
S62
BOOT
EXECUTION OF INITIALIZATION PROGRAM
S63
USER
CHANGE USER PROGRAM AFTER FWE=1
S64
USER
YES
CHECK FWE = 1 ?
NO
USER
END BY USER DEFINED ERROR PROCESS
S65
PREPARATION OF DATA TO BE PROGRAMMED
USER
REPEAT UNTIL PROCESSING OF THE PURPOSE IS COMPLETED
EXECUTION OF PROGRAMMING/ERASE
S66
END
PROGRAMMING/ERASE INITIALIZATION PROCESS
OPERATION IN USER MAT/OPERATION IN INTERNAL RAM
RELEASE OF PROGRAMMING/ERASE HARD WARE PROTECTION
OPERATION IN USER MAT/OPERATION IN INTERNAL RAM
EXECUTION OF PROGRAMMING/ERASE
OPERATION IN INTERNAL RAM

FIG. 14

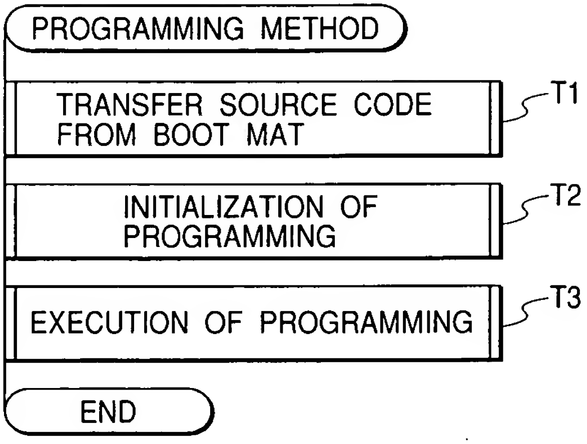

PROGRAMMING METHOD
TRANSFER SOURCE CODE FROM BOOT MAT
T1
INITIALIZATION OF PROGRAMMING
T2
EXECUTION OF PROGRAMMING
T3
END

FIG. 15

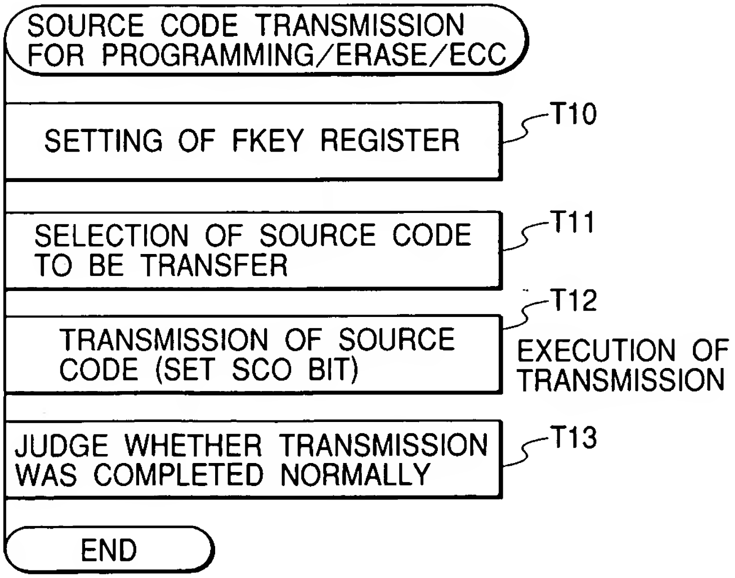

SOURCE CODE TRANSMISSION FOR PROGRAMMING/ERASE/ECC
SETTING OF FKEY REGISTER
T10
SELECTION OF SOURCE CODE TO BE TRANSFER
T11
TRANSMISSION OF SOURCE CODE (SET SCO BIT)
T12
EXECUTION OF TRANSMISSION
JUDGE WHETHER TRANSMISSION WAS COMPLETED NORMALLY
T13
END

FIG. 16

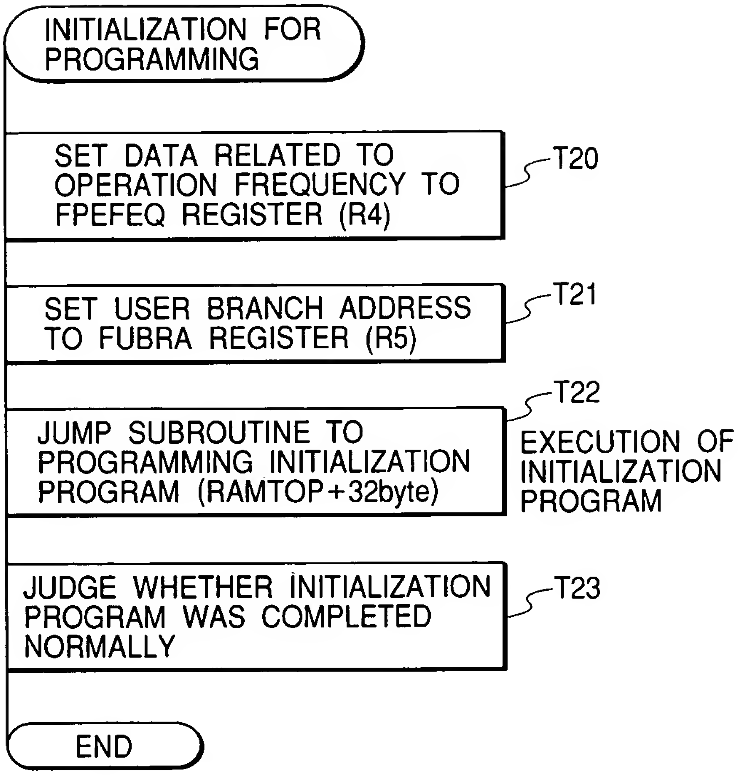

INITIALIZATION FOR PROGRAMMING
SET DATA RELATED TO OPERATION FREQUENCY TO FPEFEQ REGISTER (R4)
T20
SET USER BRANCH ADDRESS TO FUBRA REGISTER (R5)
T21
T22
JUMP SUBROUTINE TO PROGRAMMING INITIALIZATION PROGRAM (RAMTOP+32byte)
EXECUTION OF INITIALIZATION PROGRAM
JUDGE WHETHER INITIALIZATION PROGRAM WAS COMPLETED NORMALLY
T23
END

FIG. 17

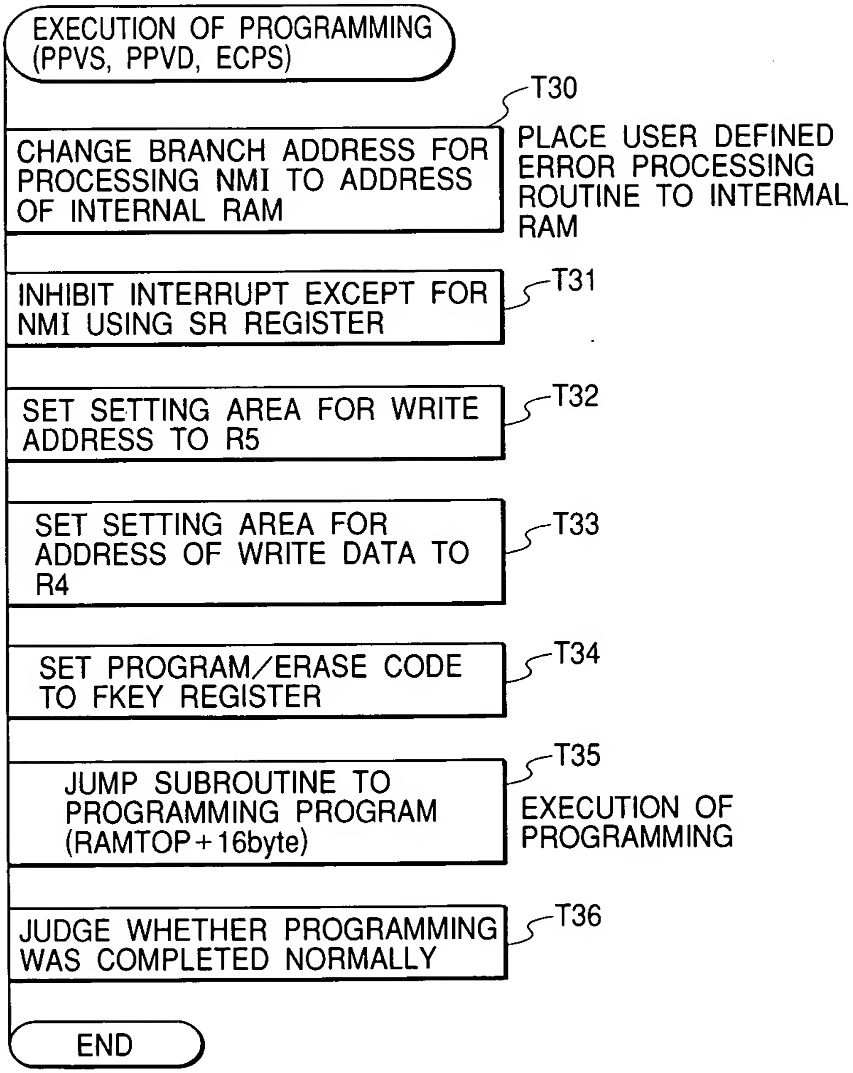

EXECUTION OF PROGRAMMING (PPVS, PPVD, ECPS)
T30
CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM
PLACE USER DEFINED ERROR PROCESSING ROUTINE TO INTERMAL RAM
T31
INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER
T32
SET SETTING AREA FOR WRITE ADDRESS TO R5
T33
SET SETTING AREA FOR ADDRESS OF WRITE DATA TO R4
T34
SET PROGRAM/ERASE CODE TO FKEY REGISTER
T35
JUMP SUBROUTINE TO PROGRAMMING PROGRAM (RAMTOP+16byte)
EXECUTION OF PROGRAMMING
T36
JUDGE WHETHER PROGRAMMING WAS COMPLETED NORMALLY
END

FIG. 18

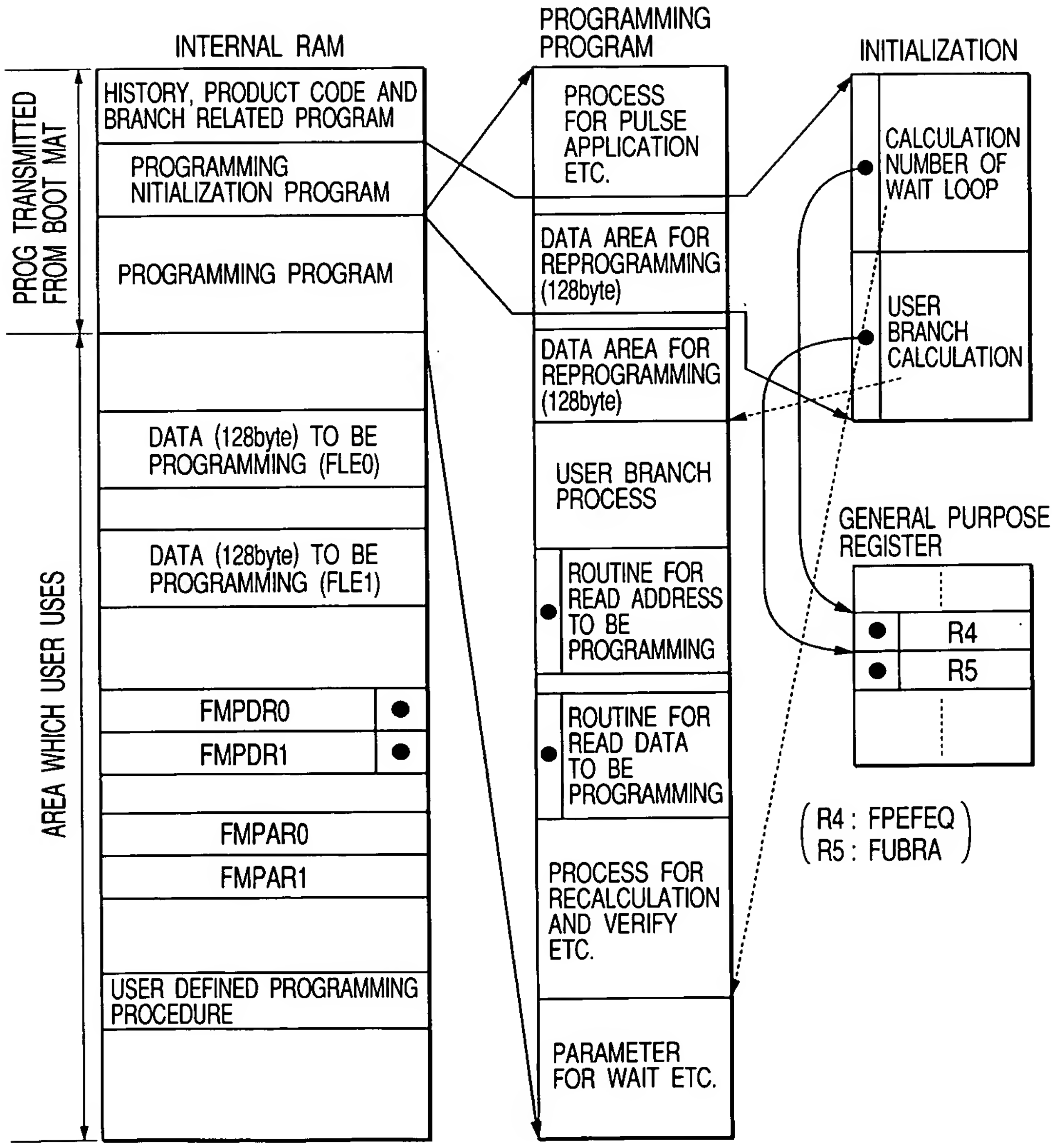

INTERNAL RAM
PROG TRANSMITTED FROM BOOT MAT
AREA WHICH USER USES
HISTORY, PRODUCT CODE AND BRANCH RELATED PROGRAM
PROGRAMMING NITIALIZATION PROGRAM
PROGRAMMING PROGRAM
DATA (128byte) TO BE PROGRAMMING (FLE0)
DATA (128byte) TO BE PROGRAMMING (FLE1)
FMPDR0
FMPDR1
FMPAR0
FMPAR1
USER DEFINED PROGRAMMING PROCEDURE
PROGRAMMING PROGRAM
PROCESS FOR PULSE APPLICATION ETC.
DATA AREA FOR REPROGRAMMING (128byte)
DATA AREA FOR REPROGRAMMING (128byte)
USER BRANCH PROCESS
ROUTINE FOR READ ADDRESS TO BE PROGRAMMING
ROUTINE FOR READ DATA TO BE PROGRAMMING
PROCESS FOR RECALCULATION AND VERIFY ETC.
PARAMETER FOR WAIT ETC.
INITIALIZATION
CALCULATION NUMBER OF WAIT LOOP
USER BRANCH CALCULATION
GENERAL PURPOSE REGISTER
R4
R5
R4 : FPEFEQ
R5 : FUBRA

FIG. 19

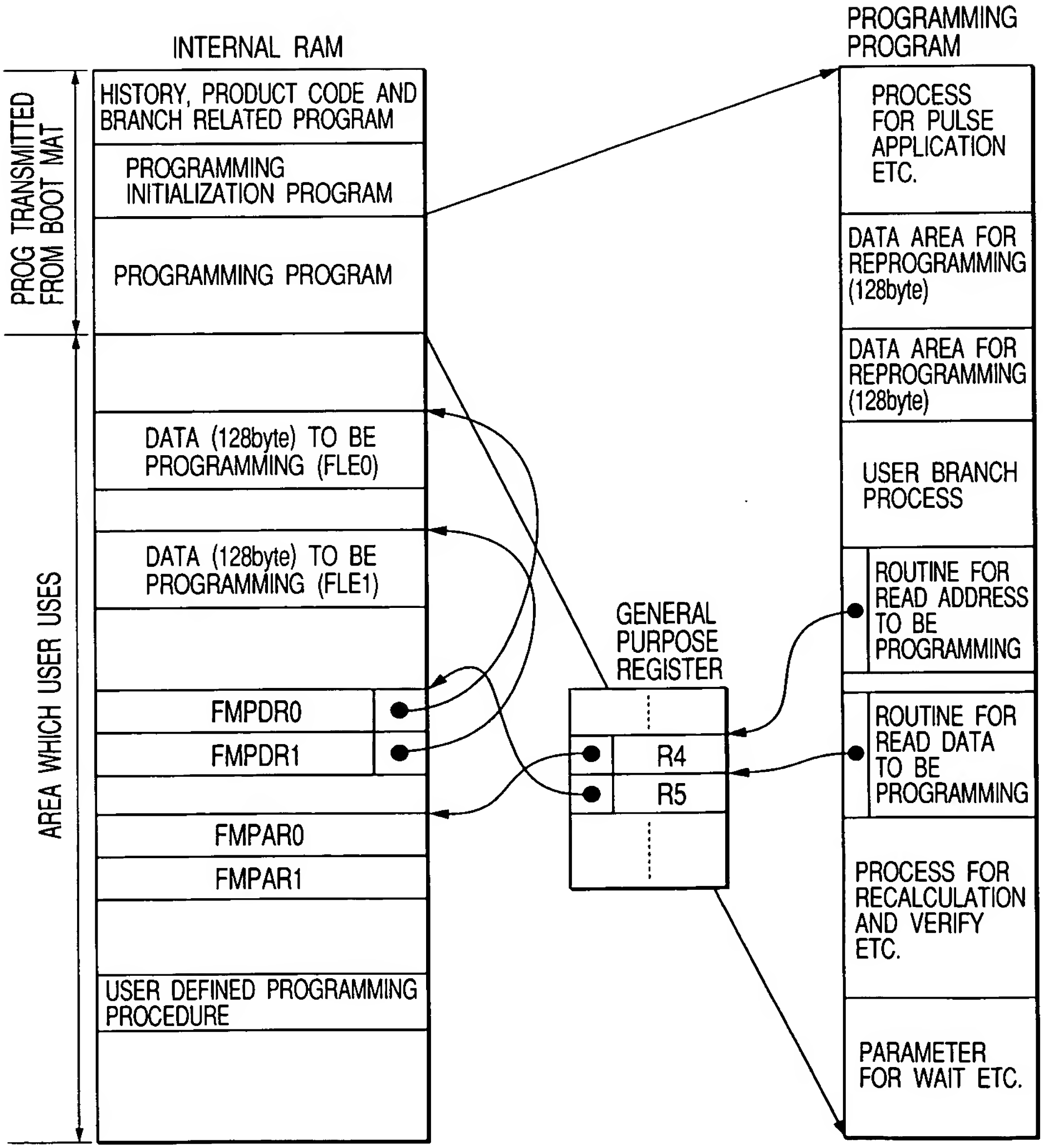

INTERNAL RAM
PROG TRANSMITTED FROM BOOT MAT
AREA WHICH USER USES
HISTORY, PRODUCT CODE AND BRANCH RELATED PROGRAM
PROGRAMMING INITIALIZATION PROGRAM
PROGRAMMING PROGRAM
DATA (128byte) TO BE PROGRAMMING (FLE0)
DATA (128byte) TO BE PROGRAMMING (FLE1)
FMPDR0
FMPDR1
FMPAR0
FMPAR1
USER DEFINED PROGRAMMING PROCEDURE
GENERAL PURPOSE REGISTER
R4
R5
PROGRAMMING PROGRAM
PROCESS FOR PULSE APPLICATION ETC.
DATA AREA FOR REPROGRAMMING (128byte)
DATA AREA FOR REPROGRAMMING (128byte)
USER BRANCH PROCESS
ROUTINE FOR READ ADDRESS TO BE PROGRAMMING
ROUTINE FOR READ DATA TO BE PROGRAMMING
PROCESS FOR RECALCULATION AND VERIFY ETC.
PARAMETER FOR WAIT ETC.

FIG. 20

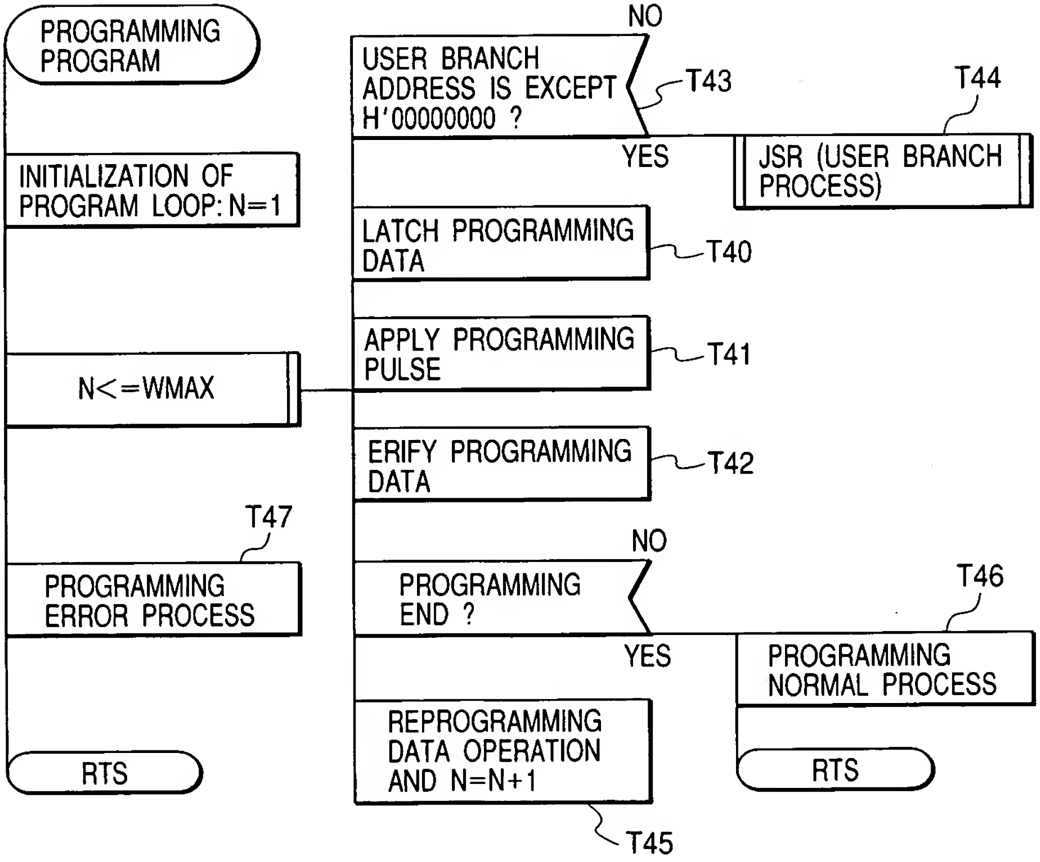

PROGRAMMING PROGRAM
INITIALIZATION OF PROGRAM LOOP: N=1
N<=WMAX
T47
PROGRAMMING ERROR PROCESS
RTS
NO
USER BRANCH ADDRESS IS EXCEPT H'00000000 ?
T43
YES
T44
JSR (USER BRANCH PROCESS)
LATCH PROGRAMMING DATA
T40
APPLY PROGRAMMING PULSE
T41
ERIFY PROGRAMMING DATA
T42
NO
PROGRAMMING END ?
YES
T46
PROGRAMMING NORMAL PROCESS
RTS
REPROGRAMMING DATA OPERATION AND N=N+1
T45

FIG. 21

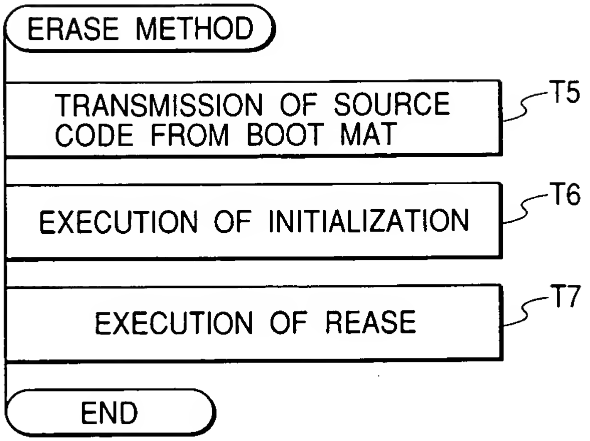

ERASE METHOD
TRANSMISSION OF SOURCE CODE FROM BOOT MAT
T5
EXECUTION OF INITIALIZATION
T6
EXECUTION OF REASE
T7
END

FIG. 22

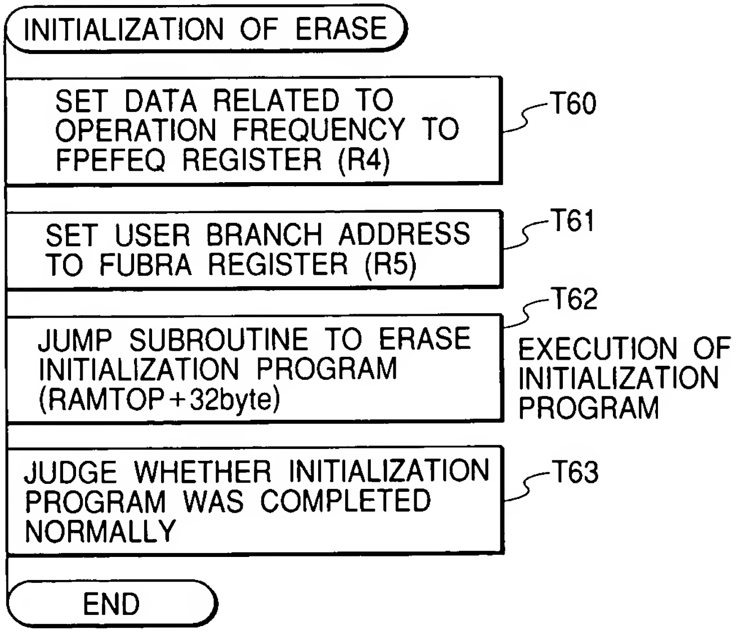

INITIALIZATION OF ERASE
SET DATA RELATED TO OPERATION FREQUENCY TO FPEFEQ REGISTER (R4)
T60
SET USER BRANCH ADDRESS TO FUBRA REGISTER (R5)
T61
JUMP SUBROUTINE TO ERASE INITIALIZATION PROGRAM (RAMTOP+32byte)
T62
EXECUTION OF INITIALIZATION PROGRAM
JUDGE WHETHER INITIALIZATION PROGRAM WAS COMPLETED NORMALLY
T63
END

FIG. 23

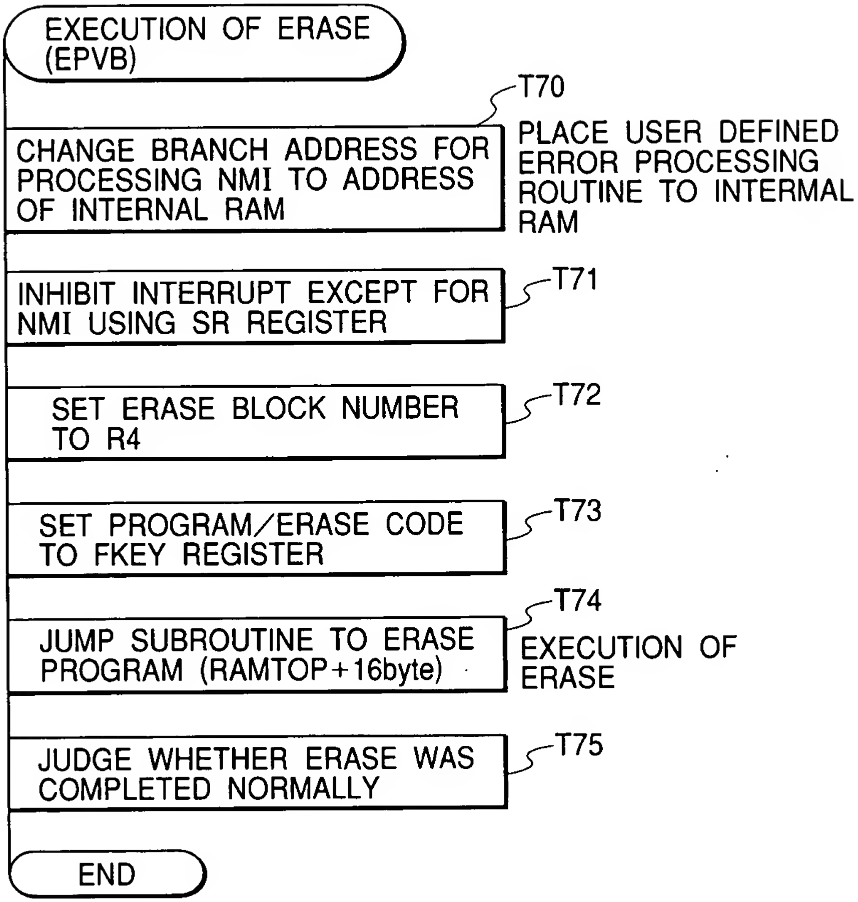

EXECUTION OF ERASE (EPVB)
T70
CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM
PLACE USER DEFINED ERROR PROCESSING ROUTINE TO INTERMAL RAM
T71
INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER
T72
SET ERASE BLOCK NUMBER TO R4
T73
SET PROGRAM/ERASE CODE TO FKEY REGISTER
T74
JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte)
EXECUTION OF ERASE
T75
JUDGE WHETHER ERASE WAS COMPLETED NORMALLY
END

FIG. 24

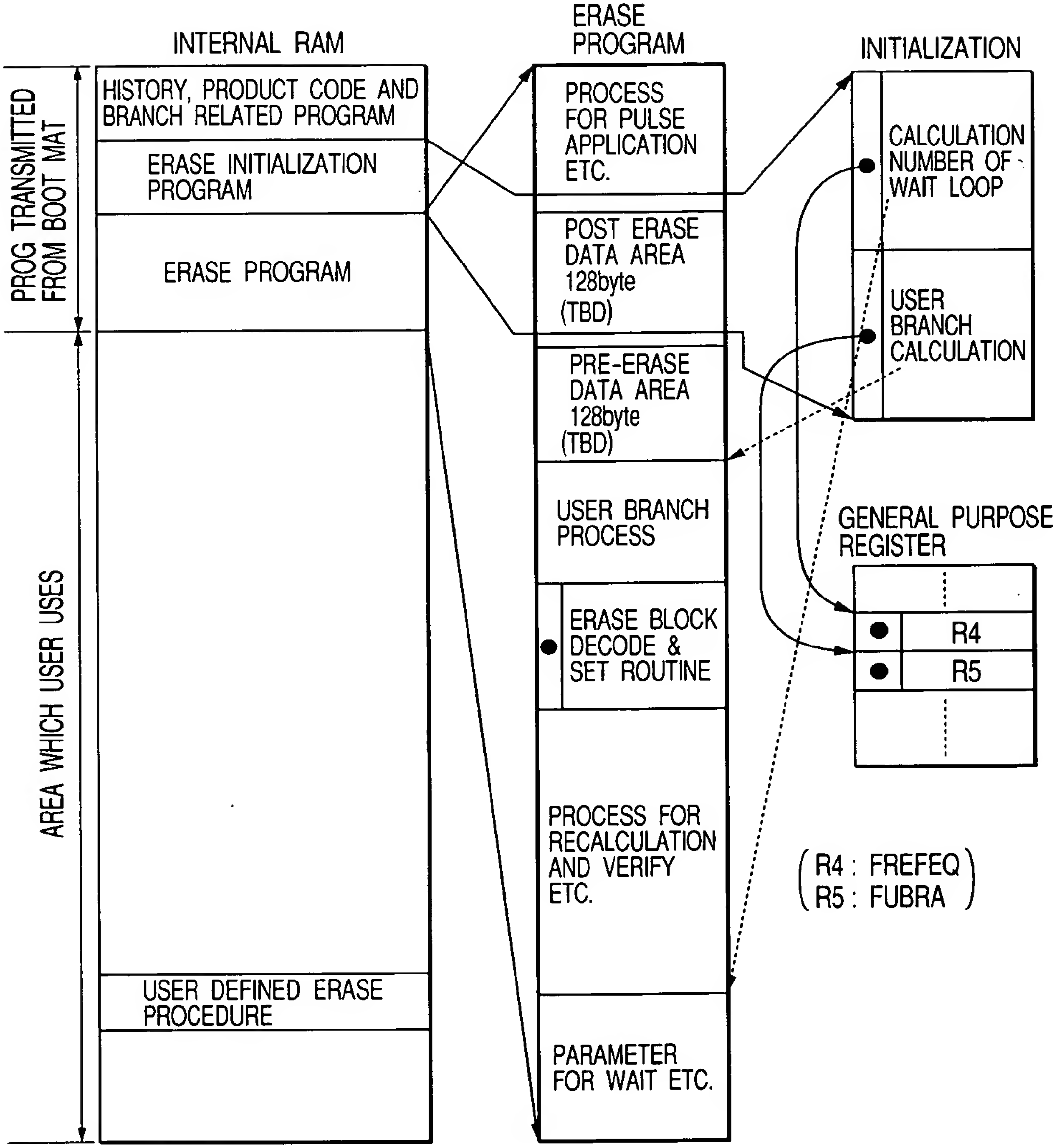

INTERNAL RAM
PROG TRANSMITTED FROM BOOT MAT
AREA WHICH USER USES
HISTORY, PRODUCT CODE AND BRANCH RELATED PROGRAM
ERASE INITIALIZATION PROGRAM
ERASE PROGRAM
USER DEFINED ERASE PROCEDURE
ERASE PROGRAM
PROCESS FOR PULSE APPLICATION ETC.
POST ERASE DATA AREA 128byte (TBD)
PRE-ERASE DATA AREA 128byte (TBD)
USER BRANCH PROCESS
ERASE BLOCK DECODE & SET ROUTINE
PROCESS FOR RECALCULATION AND VERIFY ETC.
PARAMETER FOR WAIT ETC.
INITIALIZATION
CALCULATION NUMBER OF WAIT LOOP
USER BRANCH CALCULATION
GENERAL PURPOSE REGISTER
R4
R5
R4 : FREFEQ
R5 : FUBRA

FIG. 25

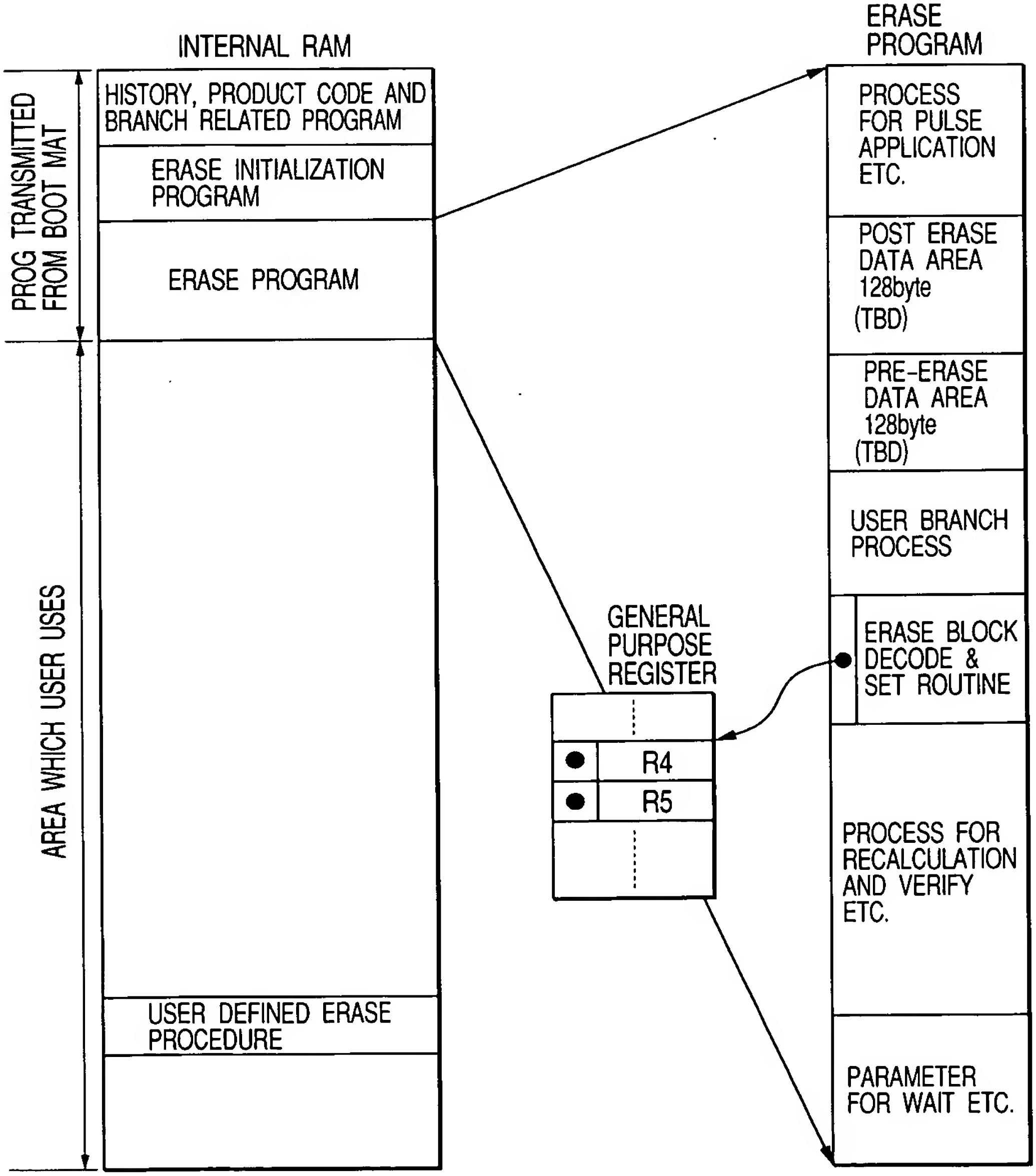

INTERNAL RAM
PROG TRANSMITTED FROM BOOT MAT
HISTORY, PRODUCT CODE AND BRANCH RELATED PROGRAM
ERASE INITIALIZATION PROGRAM
ERASE PROGRAM
AREA WHICH USER USES
USER DEFINED ERASE PROCEDURE
GENERAL PURPOSE REGISTER
R4
R5
ERASE PROGRAM
PROCESS FOR PULSE APPLICATION ETC.
POST ERASE DATA AREA 128byte (TBD)
PRE-ERASE DATA AREA 128byte (TBD)
USER BRANCH PROCESS
ERASE BLOCK DECODE & SET ROUTINE
PROCESS FOR RECALCULATION AND VERIFY ETC.
PARAMETER FOR WAIT ETC.

FIG. 26

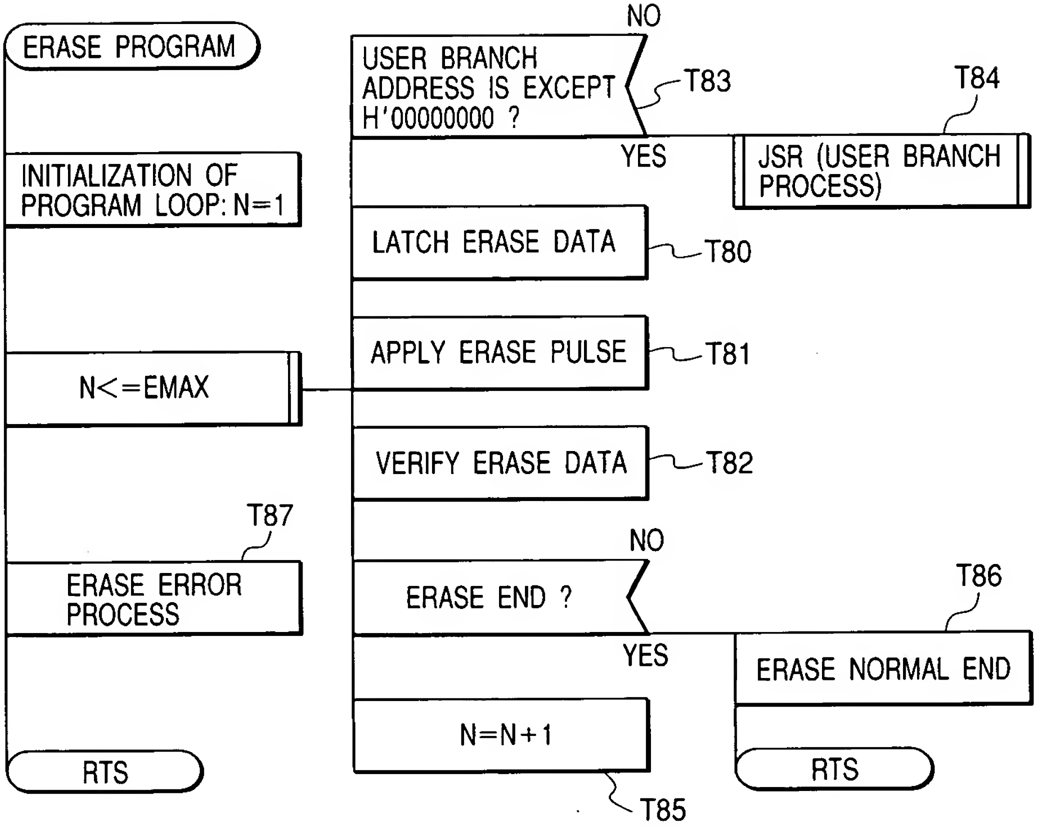
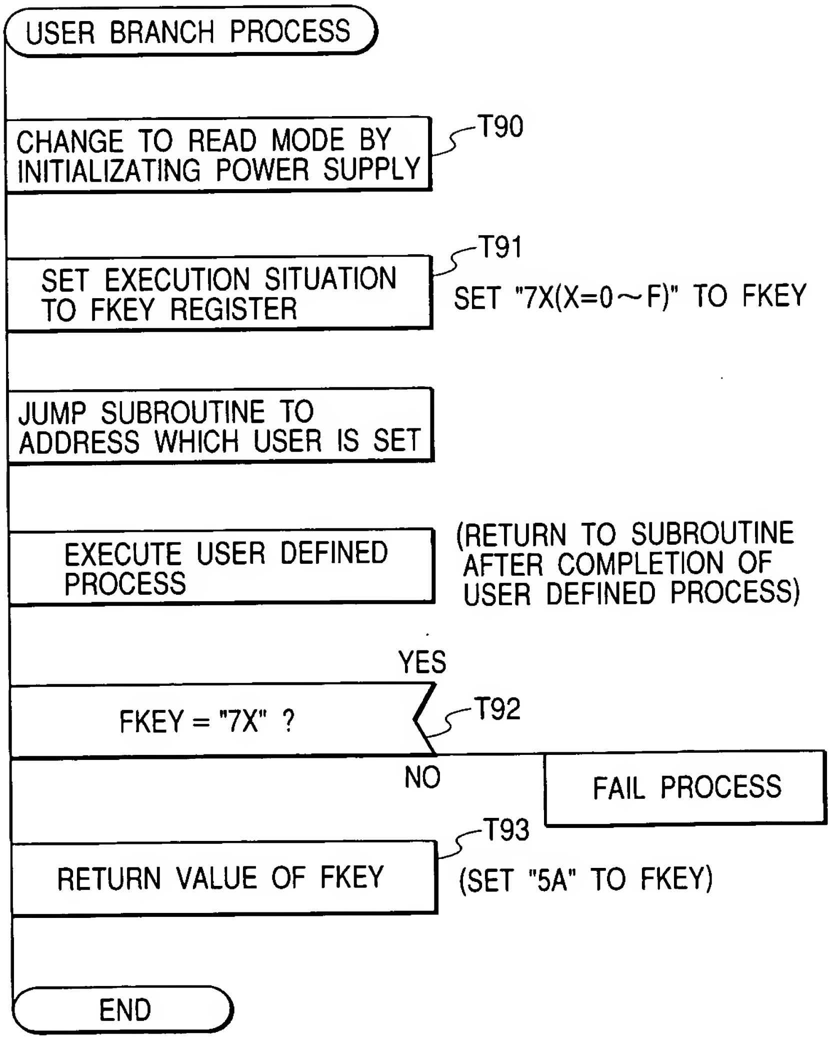

ERASE PROGRAM
INITIALIZATION OF PROGRAM LOOP: N=1
N<=EMAX
T87
ERASE ERROR PROCESS
RTS
NO
USER BRANCH ADDRESS IS EXCEPT H'00000000 ?
T83
T84
YES
JSR (USER BRANCH PROCESS)
LATCH ERASE DATA
T80
APPLY ERASE PULSE
T81
VERIFY ERASE DATA
T82
NO
ERASE END ?
T86
YES
ERASE NORMAL END
N=N+1
T85
RTS

FIG. 27


USER BRANCH PROCESS
CHANGE TO READ MODE BY INITIALIZATING POWER SUPPLY
T90
SET EXECUTION SITUATION TO FKEY REGISTER
T91
SET "7X(X=0~F)" TO FKEY
JUMP SUBROUTINE TO ADDRESS WHICH USER IS SET
EXECUTE USER DEFINED PROCESS
(RETURN TO SUBROUTINE AFTER COMPLETION OF USER DEFINED PROCESS)
YES
FKEY = "7X" ?
T92
NO
FAIL PROCESS
T93
RETURN VALUE OF FKEY
(SET "5A" TO FKEY)
END